IDEC Chip Design Contest

Brain-Computer Interface SoC with High-Throughput Neural Signal Processing Unit

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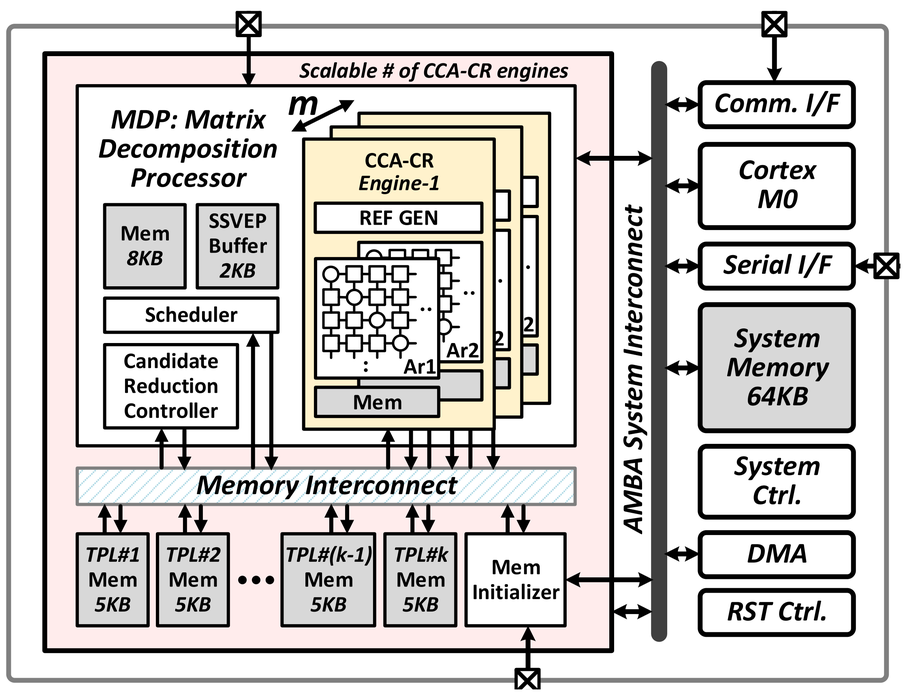
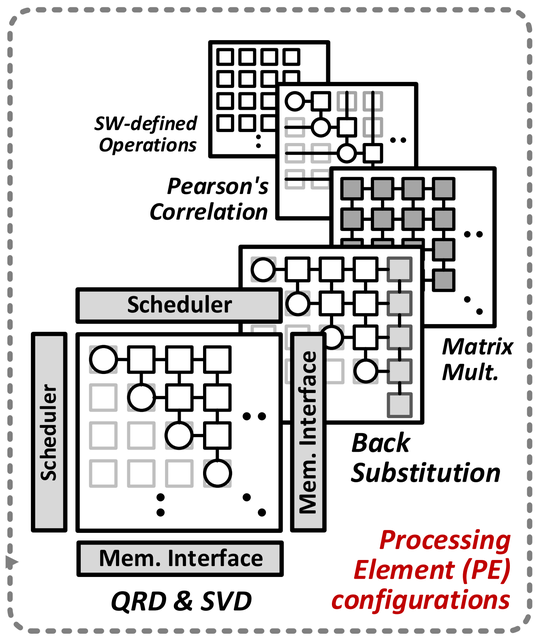
Introduction

Steady-state visual evoked potential (SSVEP) based wearable brain-computer interface (BCI) have been widely studied to enable paralyzed patients to communicate with others. However, target identification accuracy and information transfer rate (ITR), which are general performance indicators of SSVEP-based BCI system, still need to be further improved in wearable devices. In this work, we propose 8-channel SSVEP-based visual target identification system-on-chip (SoC) to improve the ITR for low-cost wearable BCI device while reducing the computational complexity dramatically without accuracy degradation. The proposed target identification algorithm, CCA-CR based on canonical correlation analysis (CCA), includes algorithmic optimizations and candidate reduction (CR) method to reduce the signal processing load by at least 75% without degrading target identification accuracy and ITR. This paper also proposes matrix decomposition processor (MDP) that computes complex matrix arithmetic operations through systolic array based CCA-CR engines. The proposed chip was fabricated in 65nm CMOS technology and operates at 50MHz 1.2V.

Proposed Architecture

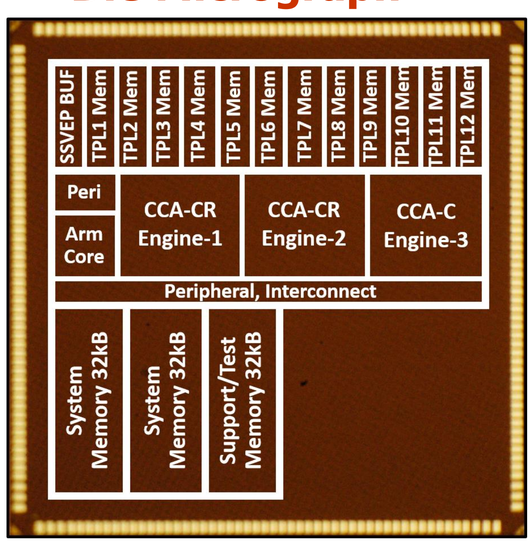




- **Implementation of proposed CCA-CR acceleration architecture:** candidate reduction (CR) based optimized CCA-Comb algorithm was proposed and implemented through suitable microarchitecture with 3 CCA-CR engines (each has 2 arrays)
- **Digit-Serial Arithmetic PE:** each PE (processing element) performs 4-bit digit serial arithmetic for low area

Chip Implementation and Results

Die Micrograph



- **Die size: 4x4mm²**
- **3 engines (6 arrays)**
- **8x8 PE array**
- **Area optimized arch.**
- **Digit serial ALU in PE**
- **12 memory banks for subject-specific EEG template data of 12 visual targets**

Chip Implementation

	Chip Information
Technology	65nm CMOS
Operating Frequency, Voltage, Core Area	50 MHz, 1.2V(core), 3.5x3.5 mm²
Circuit Type	Digital (Cell-based) Design
On-Chip Memory	158kB

This work proposes 8-channel SSVEP target identification SoC with CCA-CR, which reduces the number of CCA-Comb calculations by 75% without degrading target identification accuracy and ITR. Thanks to the multi-channel SSVEP, the SSVEP recording time is short, resulting in a significantly reduced target identification latency and a 63% increase in ITR.

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